Amendments to the Specification:

Please replace the paragraph beginning on page 5, line 27 through page 6, line 12 with the following amended paragraph:

The master 115a is typical of all the masters 115a-115d, and includes a transmitter 130 that receives a Master Tx clock signal from a phase lock loop (PLL) 132. A reference voltage controlled oscillator (VCO) 134 controls the phase lock loop 132 in each of the masters 115a-115d. The output of the transmitter 130 is connected to the near end of the channel 110a. The master 115a further includes a receiver 136 having its input connected to the near end of the channel 110a. The receiver 136 includes an analog-to-digital (A/D) converter 138 with its input constituting the receiver input, a signal processor 140 connected to the output of the A/D converter 138, and a clock recovery circuit 142. The clock recovery circuit 142 generates a Master Rx clock from the output of the signal processor 140, the Master Rx clock signal controlling the signal processor 140 and the analog-to-digital converter 138. The signal processor 140 performs functions required by the clock recovery circuit 142, for example, such as peak detection. Other signal processing, such ~~a~~ error correction for example, may be performed by a down-stream signal processor 144.

Please replace the paragraph beginning on page 11, line 11 with the following amended paragraph:

In the preferred embodiment, delaying the Slave Tx clock signal is facilitated by providing a controllable device as the delay element 232 in the slave 120a. The controllable delay element 232 is governed by a delay (next avoider) controller 260 in the slave 120a. The delay controller 260 responds to a delay command transmitted over the channel 110a by the master 115a. The problem is how to determine the optimum delay command that best minimizes the effects of NEXT/echo ~~and echo~~ noise.

Please replace the paragraph beginning on page 13, line 26 through page 14, line 11 with the following amended paragraph:

The metric processor 270, in a first embodiment, outputs a metric signal whose magnitude represents a metric corresponding to the separation distance of FIG. 3C. In this first embodiment, the metric processor 270 generates N equally spaced clocks that are derived from its local clock input. Each of these N clocks is sampled by the output of a slicer 310 of the signal processor 140, producing an N-element vector of 0's and 1's. Many, say 64, of these N-element vectors are summed, producing another N-element vector of sums or amplitudes. Then, the metric processor intelligently sorts the N cumulative amplitudes into two groups of N/2 consecutive cumulative amplitudes. There are N possible groupings, but the processor 270 selects the one grouping having the greatest contrast between the two groups. In the preferred embodiment, this contrast is the difference

between the sums of the cumulative amplitudes of each group. Preferably, this difference is the metric signal produced by the metric processor 270. In an alternative embodiment, the contrast is ~~the difference~~ a ratio between the sums of the cumulative amplitudes of each group, and this ~~difference~~ ratio is output as the metric signal.